intel®

1702A

2K (256 x 8) UV ERASABLE PROM

1702A-2	0.65 us Max.
1702A	1.0 us Max.
1702A-6	1.5 us Max.

- **Fast Access Time: Max. 650 ns (1702A–2)**
- **Fast Programming: 2 Minutes for all 2048 Bits**
- **All 2048 Bits Guaranteed* Programmable: 100% Factory Tested**

- **Static MOS: No Clocks Required**
- **Inputs and Outputs DTL and TTL Compatible**
- **Three-State Output: OR-tie Capability**

The 1702A is a 256 word by 8-bit electrically programmable ROM ideally suited for uses where fast turn-around and pattern experimentation are important. The 1702A undergoes complete programming and functional testing prior to shipment, thus insuring 100% programmability.

Initially all 2048 bits of the 1702A are in the "0" state (output low). Information is introduced by selectively programming "1"s (output high) in the proper bit location. The 1702A is packaged in a 24 pin dual in-line package with a transparent lid. The transparent lid allows the user to expose the 1702A to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device.

The circuitry of the 1702A is completely static. No clocks are required. Access times from 650ns to 1.5μs are available. A 1702AL family is available (see 1702AL data sheets for specifications) for those systems requiring lower power dissipation than the 1702A.

The 1702A is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

*Intel's liability shall be limited to replacing any unit which fails to program as desired.

PIN CONFIGURATION

A_2	1	24	V_{DD}
A_1	2	23	V_{CC}
A_0	3	22	V_{CC}
*DATA OUT 1	4 (LSB)	21	A_3
*DATA OUT 2	5	20	A_4
*DATA OUT 3	6	19	A_5
*DATA OUT 4	7	18	A_6
*DATA OUT 5	8	17	A_7
*DATA OUT 6	9	16	V_{GG}
*DATA OUT 7	10	15	V_{BB}
*DATA OUT 8	11 (MSB)	14	$\overline{CS}$
V_{CC}	12	13	PROGRAM
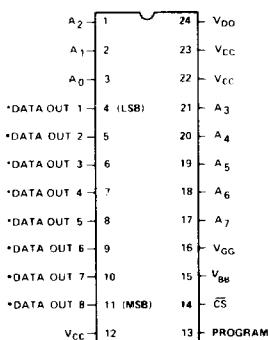
*THIS PIN IS THE DATA INPUT LEAD DURING PROGRAMMING

PIN NAMES

A_0–A_7	Address Inputs
$\overline{CS}$	Chip Select Input
D_{OUT1}–D_{OUT8}	Data Outputs

BLOCK DIAGRAM
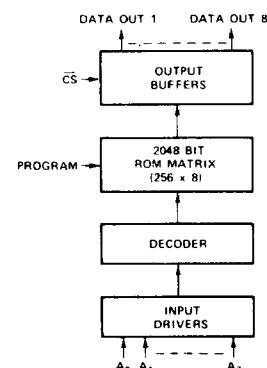
NOTE: In the read mode a logic 1 at the address inputs and data outputs is a high and logic 0 is a low.

U.S. Patent No. 3660819

PIN CONNECTIONS

The external lead connections to the 1702A differ, depending on whether the device is being programmed or used in read mode (see following table). In the programming mode, the data inputs 1-8 are pins 4-11 respectively. *The programming voltages and timing are shown in the Data Catalog ROM and PROM Programming Instructions section.*

MODE \ PIN	12 (V_CC)	13 (Program)	14 ($\overline{CS}$)	15 (V_BB)	16 (V_GG)	22 (V_CC)	23 (V_CC)	24 (V_DD)
Read	V_{CC}	V_{CC}	GND	V_{CC}	V_{GG}	V_{CC}	V_{CC}	V_{DD}
Programming	GND	Program Pulse	GND	V_{BB}	Pulsed V_{GG}	GND	GND	Pulsed V_{DD}

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . $-10°C$ to $+80°C$
Storage Temperature . . . . $-65°C$ to $+125°C$
Soldering Temperature of Leads (10 sec) . . . . $+300°C$
Power Dissipation . . . . 2 Watts
Read Operation: Input Voltages and Supply
  Voltages with respect to V_{CC} . . . . $+0.5V$ to $-20V$
Program Operation: Input Voltages and Supply
  Voltages with respect to V_{CC} . . . . $-48V$

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

$T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, $V_{DD} = -9V \pm 5\%$, $V_{GG} = -9V \pm 5\%$, unless otherwise noted.

READ OPERATION

Symbol	Test	1702A, 1702A-6 Limits			1702A-2 Limits			Unit	Conditions
		Min.	Typ.[1]	Max.	Min.	Typ.[1]	Max.		
I_{LI}	Address and Chip Select Input Load Current			1			1	μA	$V_{IN} = 0.0V$
I_{LO}	Output Leakage Current			1			1	μA	$V_{OUT} = 0.0V$, $\overline{CS} = V_{IH2}$
I_{DD1}[1]	Power Supply Current		35	50		40	60	mA	$\overline{CS} = V_{IH2}$, $I_{OL} = 0.0mA$, $T_A = 25°C$, Continuous
I_{DD2}	Power Supply Current		32	46		37	55	mA	$\overline{CS} = 0.0V$, $I_{OL} = 0.0mA$, $T_A = 25°C$, Continuous
I_{DD3}	Power Supply Current		38	60		43	65	mA	$\overline{CS} = V_{IH2}$, $I_{OL} = 0.0mA$, $T_A = 0°C$, Continuous
I_{CF1}	Output Clamp Current		8	14		7	13	mA	$V_{OUT} = -1.0V$, $T_A = 0°C$, Continuous
I_{CF2}	Output Clamp Current		7	13		6	12	mA	$V_{OUT} = -1.0V$, $T_A = 25°C$, Continuous
I_{GG}	Gate Supply Current			1			1	μA	
V_{IL1}	Input Low Voltage for TTL Interface	-1		0.65	-1		0.65	V	
V_{IL2}	Input Low Voltage for MOS Interface	V_{DD}		$V_{CC}-6$	V_{DD}		$V_{CC}-6$	V	
V_{IH1}	Addr. Input High Voltage	$V_{CC}-2$		$V_{CC}+0.3$	$V_{CC}-2$		$V_{CC}+0.3$	V	
V_{IH2}	Chip Sel. Input High Volt.	$V_{CC}-2$		$V_{CC}+0.3$	$V_{CC}-1.5$		$V_{CC}+0.3$	V	
I_{OL}	Output Sink Current	1.6	4		1.6	4		mA	$V_{OUT} = 0.45V$
I_{OH}	Output Source Current	-2.0			-2.0			mA	$V_{OUT} = 0.0V$
V_{OL}	Output Low Voltage		-3	0.45		-3	0.45	V	$I_{OL} = 1.6mA$
V_{OH}	Output High Voltage	3.5	4.5		3.5	4.5		V	$I_{OH} = -200\mu A$

Note 1: Typical values are at nominal voltages and $T_A = 25°C$.

A.C. Characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$, $V_{DD} = -9V \pm 5\%$, $V_{GG} = -9V \pm 5\%$ unless otherwise noted

Symbol	Test	1702A Limits		1702A-2 Limits		1702A-6 Limits		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Freq.	Repetition Rate		1		1.6		0.66	MHz
t_{OH}	Previous Read Data Valid	0.1		0.1		0.1		μs
t_{ACC}	Address to Output Delay		1		0.65		1.5	μs
t_{CS}	Chip Select Delay	0.1		0.3		0.6		μs
t_{CO}	Output Delay From $\overline{CS}$		0.9		0.35		0.9	μs
t_{OD}	Output Deselect		0.3		0.3		0.3	μs

PROM/ROM

Capacitance * $T_A = 25°C$

| SYMBOL	TEST	TYPICAL	MAXIMUM	UNIT	CONDITIONS
C_{IN}	Input Capacitance	8	15	pF	$V_{IN} = V_{CC}$ ⎤ All $\overline{CS} = V_{CC}$ ⎥ unused pins
C_{OUT}	Output Capacitance	10	15	pF	$V_{OUT} = V_{CC}$ ⎥ are at A.C. $V_{GG} = V_{CC}$ ⎦ ground

*This parameter is periodically sampled and is not 100% tested.

Switching Characteristics

Conditions of Test:
Input pulse amplitudes: 0 to 4V; t_R, t_F ≤ 50 ns
Output load is 1 TTL gate; measurements made
at output of TTL gate ($t_{PD} \leq 15$ ns), $C_L = 15$pF

A) READ OPERATION
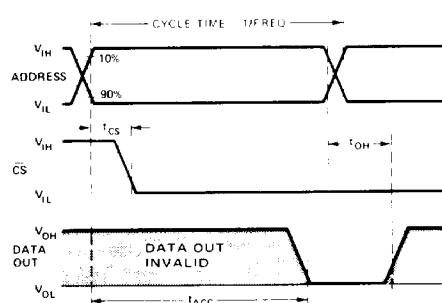
B) DESELECTION OF DATA OUTPUT IN OR-TIE OPERATION
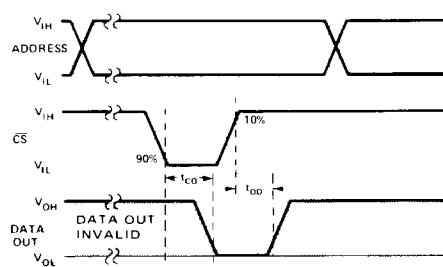
Typical Characteristics

PROM/ROM

OUTPUT CURRENT VS. V_DD SUPPLY VOLTAGE

$V_{CC} = +5V$
$V_{GG} = -9V$
$V_{OL} = +.45V$
$T_A = 25°C$

Specified Operating Range

$V_{CC} = +5V$
$V_{GG} = -9V$
$V_{OH} = 0.0V$
$T_A = 25°C$

I_OL OUTPUT SINK CURRENT (mA)
I_OH OUTPUT SOURCE CURRENT (mA)
V_DD SUPPLY VOLTAGE (V)
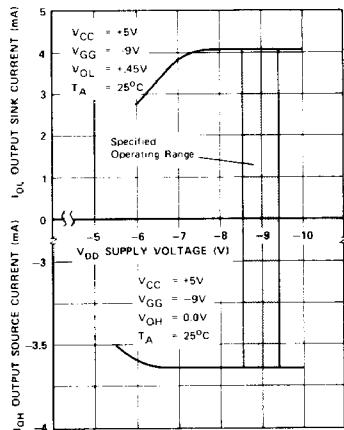
OUTPUT CURRENT VS. TEMPERATURE

$V_{CC} = +5V$
$V_{DD} = -9V$
$V_{GG} = -9V$
$V_{OL} = +.45V$

$\overline{CS} = 0.0V$

$V_{CC} = +5V$
$V_{DD} = -9V$
$V_{GG} = -9V$
$V_{OH} = 0.0V$

$\overline{CS} = 0.0V$

I_OL OUTPUT SINK CURRENT (mA)
I_OH OUTPUT SOURCE CURRENT (mA)
AMBIENT TEMPERATURE (°C)
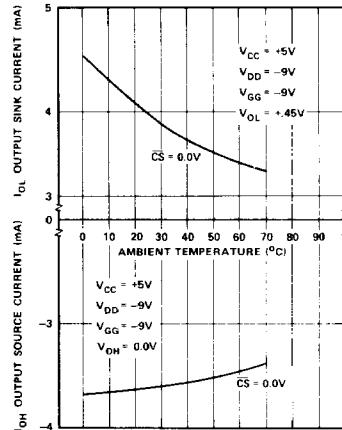
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE

$V_{CC} = +5V$
$V_{DD} = -9V$
$V_{GG} = -9V$
$T_A = 25°C$

$\overline{CS} = 0.0V$

I_OL OUTPUT SINK CURRENT (mA)
OUTPUT VOLTAGE (VOLTS)

I_DD CURRENT VS. TEMPERATURE

$V_{CC} = +5V$
$V_{DD} = -9V$
$V_{GG} = -9V$
INPUTS = V_{CC}
OUTPUTS ARE OPEN

$\overline{CS} = V_{CC}$

$\overline{CS} = 0.0V$
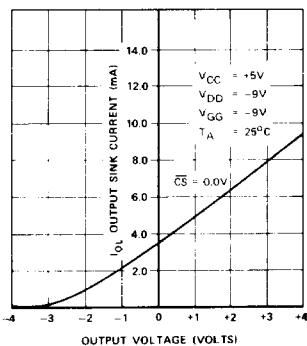
I_DD CURRENT (mA)
AMBIENT TEMPERATURE (°C)
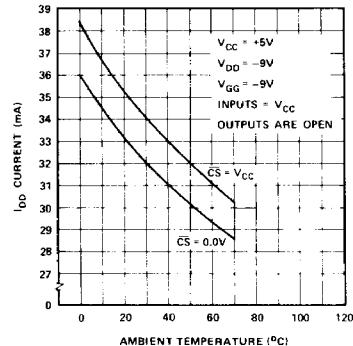
ACCESS TIME VS. LOAD CAPACITANCE

1702A
1 TTL LOAD
$V_{CC} = +5V$
$V_{DD} = -9V$
$V_{GG} = -9V$
$T_A = 25 C$
1702A-2

ACCESS TIME (ns)
LOAD CAPACITANCE (pF)
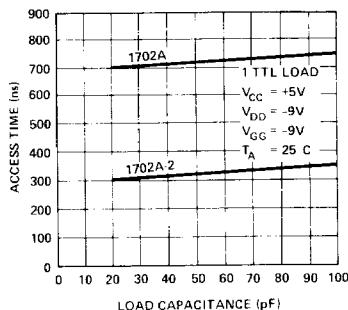
ACCESS TIME VS. TEMPERATURE

1702A
1 TTL LOAD = 20 pF
$V_{CC} = +5V$
$V_{DD} = -9V$
$V_{GG} = -9V$
1702A-2

ACCESS TIME (ns)
AMBIENT TEMPERATURE (C)